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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,783	03/25/2004	Long-Hui Lin	LKSP0026USA	2782

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NORTH AMERICA INTERNATIONAL PATENT OFFICE (NAIPC)
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
SUN, XIUQIN	
ART UNIT	**PAPER NUMBER**
2863	

DATE MAILED: 04/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/708,783	LIN, LONG-HUI	
	Examiner	Art Unit	
	Xiuqin Sun	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4, 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Steffan et al. (U.S. Pat. No. 6338001) in view of Chen et al. (U.S. Pat. No. 5862055).

In regard to claim 1:

Steffan et al. teach a method of defect control of a semiconductor process comprising following steps: providing a patterned wafer comprising a plurality of first defects (cols. 1-2, lines 36-10); performing a semiconductor process which forms a plurality of second defects on the patterned wafer (cols. 1-2, lines 36-34); performing a defect inspection to detect the plurality of first defects and second defects (cols. 1-2, lines 59-34); and classifying the detected defects into the first defects and the second defects and separating the second defects into a plurality of defect types (cols. 1-2, lines 59-49 and cols. 2-3, lines 64-2).

In regard to claims 3, 4, 6 and 7:

The teaching of Steffan et al. further includes: classifying the detected defects based on defect information wherein said defect information of each defect type comprises an influence degree over a yield of the semiconductor process of each defect type (cols. 2-3, lines 35-2); separating the second defects into killer defects and non--killer defects according to the degree of the influence degree over the yield of the semiconductor process after classifying the defects (col. 2, lines 35-63); utilizing inline automatic defect classification (ADC) tools to classify the defects (col. 2, lines 35-49); and said patterned wafer is an in-line product wafer (cols. 1-2, lines 36-10).

In regard to claims 1 and 2:

Steffan et al. do not mention expressly: separating the second defects into a plurality of defect types according to a predetermined database. Steffan et al. further do not mention: said database comprises a classifying rule of each defect type and defect information of each defect type.

Chen et al. teach a method of determining classification rules for defects occurring in semiconductor manufacturing processes (see Abstract), including: classifying detected defects into a plurality of defect types according to a predetermined database (Fig. 1 and col. 3, lines 48-67; col. 4, lines 1-4); said database comprises a classifying rule of each defect type and defect information of each defect type (col. 4, lines 47-67 and col. 5, lines 1-60).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the teaching of Chen et al. in the invention of Steffan et al. in order to make the classification of the defects configurable and flexible that can be

easily customized for a particular need (Chen et al., col. 4, lines 47-67 and col. 5, lines 1-60).

3. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Steffan et al. (U.S. Pat. No. 6338001) in view of Chen et al. (U.S. Pat. No. 5862055), as applied to claim 4 above, and further in view of Dor et al. (U.S. Pub. No. 20020072162).

Steffan et al. and Chen et al. teach a method that includes the subject matter discussed above. Steffan et al. and Chen et al. do not mention expressly: when killer defects are detected, the method further comprises following steps: performing a root cause analysis according to the defect type of the detected defects; and informing a responsible person of the semiconductor process to correct process parameters of the semiconductor process.

Dor et al. teach a method and apparatus for conducting case study of defects on semiconductor wafers (see Abstract), including: performing a root cause analysis according to the defect type of the detected defects (sections 0113, 0114, 0117 and 0126); and informing a responsible person of the semiconductor process to correct process parameters of the semiconductor process (sections 0113, 0114, 0117 and 0126).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the teaching of Dor et al. in the combination of Steffan et al. and Chen et al. in order to provide a better understanding of the wafer defects and correlate the cause of the defects with proper solutions (Dor et al., sections 0006 and 0007).

Contact Information

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Xiuqin Sun whose telephone number is (571)272-2280. The examiner can normally be reached on 6:30am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571)272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

XS

April 8, 2005

MICHAEL NGHIEM
PRIMARY EXAMINER

Xiuqin Sun
Examiner
Art Unit 2863